What is claimed is:

1. An adder to sum two binary numbers, comprising:

at least one circuit adapted to generate a group of carries;

at least one sum generator adapted to generate a pair of conditional sums; and

at least one device adapted to select between the pair of conditional sums in response to one of the group of carries.

2. The adder of claim 1, further comprising at least one second circuit adapted to generate additional carries missing from the group of carries to provide one carry for every group of a predetermined number of bits of the two binary numbers.

3. The adder of claim 2, wherein the at least one second circuit is adapted to generate two conditional carries for each additional carry and further comprising another device to select between the two conditional carries to provide each additional carry in response to one of the group of carries.

4. The adder of claim of claim 3, wherein the at least one device and the other device are each multiplexers.

5. The adder of claim 4, further comprising a multiplexer recovery circuit coupled to each of the multiplexers.

6. The adder of claim 2, wherein the at least one second circuit is an intermediate carry generator.

7. The adder of claim 1, wherein the at least one circuit is a sparse carry-merge circuit.

8. An adder to sum two binary numbers, comprising:

a sparse carry-merge circuit adapted to generate a first predetermined number of carry signals;

a plurality of intermediate carry generators each coupled to the sparse carry merge circuit and adapted to generate a second predetermined number of carry signals; and

a plurality of conditional sum generators coupled to the sparse carry-merge circuit and the plurality of intermediate carry generators and adapted to provide the sum of the two binary numbers.

9. The adder of claim 8, wherein the sparse carry-merge circuit merges groups of sixteen bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group.

10. The adder of claim 8, wherein the sparse carry-merge circuit merges groups of eight bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group.

11. The adder of claim 8, wherein the second predetermined number of carry signals is one carry signal for each group of four merged bits of the two binary numbers.

12. The adder of claim 8, wherein the sparse-carry merge circuit includes a plurality of stages, each stage including a plurality of carry-merge logic gates to combine adjacent output signals from a preceding stage to provide the first predetermined number of carry signals.

13. The adder of claim 8, wherein the sparse-carry merge circuit comprises: a first stage adapted to generate a plurality of first propagate signals and a first generate signal associated with each first propagate signal by merging the first binary number with the second binary number;

a second stage adapted to generate a plurality of second propagate signals and a second generate signal associated with each second propagate signal by merging adjacent pairs of each of the first propagate signals and each of the associated first generate signals;

a third stage adapted to generate a plurality of third propagate signals and a third generate signal associated with each third propagate signal by merging adjacent pairs of each of the second propagate signals and each of the associated second generate signals;

a fourth stage adapted to generate a plurality of fourth propagate signals and a fourth generate signal associated with each fourth propagate signal by merging adjacent pairs of the third plurality of propagate signals and the associated third generate signals;

a fifth stage adapted to generate a plurality of fifth propagate signals and a fifth generate signal associated with each fifth propagate signal by merging adjacent pairs of each of the fourth propagate signals and the associated fourth generate signals; and

a sixth stage adapted to generate the first predetermined number of carry signals by merging each fifth propagate signal and associated fifth generate signal with each fifth generate signal from a carry-merge logic gate of the fifth stage lower in digit order than a carry-merge logic gate of the sixth stage performing the merge operation, wherein a fifth generate signal from a last carry-merge gate in decreasing digit order is inverted to provide one of the first predetermined number of carry signals.

14. The adder of claim 13, wherein each of the third propagate signals and associated third generate signals are coupled to the plurality of intermediate carry generators.

15. The adder of claim 8, wherein each of the plurality of intermediate carry generators comprises three stages of ripple-carry merge gates.

16. The adder of claim 8, wherein each of the plurality of intermediate carry generators comprises a plurality of rail pairs, one rail of each rail pair being adapted to generate a first conditional carry signal for a logic 0 carry being input to the intermediate carry generator and another rail of each rail pair being adapted to generate a second conditional carry signal for a logic 1 carry being input to the intermediate carry generator.

17. The adder of claim 8, further comprising:

a first intermediate carry generator of the plurality of intermediate carry generators, including:

a first circuit adapted to generate a first carry signal of the second predetermined number of carry signals in response to a first merged propagate signal and a first merged generate signal from the sparse carry-merge circuit,

a second circuit adapted to generate a second carry signal of the second predetermined number of carry signals in response to a second merged propagate signal and a second merged generate signal from the sparse carry-merge circuit, and

a third circuit adapted to generate a third carry signal of the second predetermined number of carry signals in response to a third merged propagate signal and a third merged generate signal from the sparse carry-merge circuit;

a second intermediate carry generator of the plurality of intermediate carry generators, including:

a first circuit adapted to generate a fourth carry signal of the second predetermined number of carry signals in response to a fourth merged propagate signal and a fourth merged generate signal from the sparse carry-merge circuit,

a second circuit adapted to generate a fifth carry signal of the second predetermined number of carry signals in response to a fifth merged propagate signal and a fifth merged generate signal from the sparse carry-merge circuit, and

a third circuit adapted to generate a sixth carry signal of the second predetermined number of carry signals in response to a sixth merged propagate signal and a sixth merged generate signal from the sparse carry-merge circuit;

a third intermediate carry generator of the plurality of intermediate carry generators, including:

a first circuit adapted to generate a seventh carry signal in response to a seventh merged propagate signal and a seventh merged generate signal from the sparse carry-merge circuit,

a second circuit adapted to generate an eighth carry signal in response to an eighth merged propagate signal and an eighth merged generate signal from the sparse carry-merge circuit, and

a third circuit adapted to generate a ninth carry signal in response to a ninth merged propagate signal and a ninth merged generate signal from the sparse carry-merge circuit; and

a fourth intermediate carry generator of the plurality of intermediate carry generators, including:

a first circuit adapted to generate a tenth carry signal in response to a tenth merged propagate signal and a tenth merged generate signal from the sparse carry-merge circuit,

a second circuit adapted to generate an eleventh carry signal in response to an eleventh merged propagate signal and an eleventh merged generate signal from the sparse carry-merge circuit, and

a third circuit adapted to generate a twelfth carry signal in response to a twelfth merged propagate signal and a twelfth merged generate signal from the sparse carry-merge circuit.

18. The adder of claim 8, wherein each intermediate carrier generator comprises a plurality of circuits to each generate a carry signal of the second predetermined number of carry signals, each of the plurality of circuits including:

a first rail adapted to generate a first conditional carry,

a second rail adapted to generate a second conditional carry; and

a multiplexer adapted to select between the first conditional carry and the second conditional carry.

19. The adder of claim 8, wherein each of the plurality of conditional sum generators comprises a plurality of stages of ripple carry-merge gates and exclusive OR gates.

20. The adder circuit of claim 8, wherein each of the plurality of conditional sum generators comprises:

a first sum circuit including:

a first rail adapted to generate a first sum signal from a first propagate signal,

a second rail adapted to generate a second sum signal from the first propagate signal, and

a multiplexer adapted to select one of the first sum signal or the second sum signal in response to a first carry signal of the first or second predetermined number of carry signals;

a second sum circuit including:

a first rail adapted to generate a third sum signal, wherein the first rail of the second sum circuit includes a first carry-merge/exclusive OR logic gate to merge a second propagate signal and a second generate signal with a logic 0 carry-in,

a second rail adapted to generate a fourth sum signal, wherein the second rail of the second sum circuit includes a second combination carry-merge/exclusive OR logic gate to merge the second propagate signal and the second generate signal with a logic 1 carry-in, and

a multiplexer adapted to select between the third sum signal and the fourth sum signal in response to a second carry signal of the first and second predetermined number of carry signals;

a third sum circuit including:

a first rail adapted to generate a fifth sum signal, wherein the first rail of the third sum circuit includes a third carry-merge/exclusive OR logic gate to merge a third propagate signal and a third generate signal with an output generate signal from the first combination carry-merge/exclusive OR logic gate,

a second rail adapted to generate a sixth sum signal, wherein the second rail of the third sum circuit includes a fourth combination carry-merge/exclusive OR logic gate to merge the third propagate signal and the third generate signal with an output generate signal from the second combination carry-merge/exclusive OR gate, and

a multiplexer adapted to select between the fifth sum signal and the sixth sum signal in response to a third carry signal of the first and second predetermined number of carry signals; and

a fourth sum circuit including:

a first rail adapted to generate a seventh sum signal, wherein the first rail of the fourth sum circuit includes a fifth combination carry-merge/exclusive OR logic gate to merge a fourth propagate signal and a fourth generate signal with an output generate signal from the third combination carry-merge/exclusive OR logic gate,

a second rail adapted to generate an eighth sum signal, wherein the second rail of the fourth sum circuit includes a sixth combination carry-merge/exclusive OR logic gate to merge the fourth propagate signal and the fourth generate signal with an output generate signal from the fourth combination carry-merge/exclusive OR gate, and

a multiplexer adapted to select between the seventh sum signal and the eighth sum signal in response to a fourth carry signal of the first and second predetermined number of carry signals.

21. The adder of claim 8, further comprising a multiplexer recovery circuit coupled to the sparse carry-merge circuit, each of the plurality of intermediate carry generators and each of the plurality of conditional sum generators.

22. An electronic system, comprising:

a processor including an arithmetic logic unit, the arithmetic logic unit including at least one adder and the adder including:

a sparse carry-merge circuit adapted to generate a group of carries,

a plurality of intermediate carry generators each coupled to the sparse carry-merge circuit and adapted to generate additional carries missing from the group of carries, and

a plurality of sum generators coupled to the sparse carry-merge circuit and the plurality of intermediate carry generators and adapted to provide the sum of two binary numbers; and

a memory system coupled to the processor.

23. The electronic system of claim 22, wherein the sparse carry-merge circuit generates at least one carry for every group of sixteen input bits to the adder.

24. The electronic system of claim 22, wherein the sparse carry-merge circuit generates at least one carry for every group of eight input bits to the adder.

25. The electronic system of claim 22, wherein the intermediate carry generator generates at least one carry signal for every group of four input bits to the adder.

26. The electronic system of claim 22, wherein each of the sum generators comprises:

four dual rail sum circuits, each circuit providing one bit of a final sum and one rail generating a conditional sum for a logic 0 carry-in and the other rail generating a conditional sum for a logic 1 carry-in; and

a multiplexer coupled to each dual rail sum circuit to select the one or the other rail in response to a one in four carry from the intermediate carry generator.

27. The electronic system of claim 22, further comprising a multiplexer recovery circuit coupled to the sparse carry-merge circuit, each of the plurality of intermediate carry generators and each of the plurality of conditional sum generators.

28. A method of adding two binary numbers, comprising:

generating a first predetermined number of carries by merging bits of the two binary numbers;

generating a plurality of conditional carries for a logic 0 carry-in;

generating another plurality of conditional carries for a logic 1 carry-in;

selecting between each one of the plurality of conditional carries for a logic 0 carry-in and an associated one of the other plurality of conditional carries for a logic 1 carry-in in response to a carry-in from the first predetermined number of carries to provide a second predetermined number of carries;

generating a plurality of conditional sums for a logic 0 carry-in;

generating another plurality of conditional sums for a logic 1 carry-in;

selecting between each one of the plurality of conditional sums for the logic 0 carry-in and an associated one of the other plurality of conditional sums for the logic 1 carry-in in response to a carry-in from the first and second predetermined number of carries to provide a final sum of the two binary numbers.

29. The method of claim 28, wherein generating the first predetermined number of carries comprises generating at least one carry for every sixteen bits of the first and second binary numbers grouped from a least significant digit.

30. The method of claim 28, wherein generating the first predetermined number of carries comprises generating at least one carry for every eight bits of the first and second binary numbers grouped from a least significant digit.

31. The method of claim 28, wherein the second predetermined number of carries comprises at least one carry for every four bits of the first and second binary numbers grouped from a least significant digit.

32. The method of claim 28, comprising recovering any erroneously discharged ones of the second predetermined number of carries or digits of the final sum.

33. A method of making a processor, comprising:

forming an arithmetic logic unit;

forming at least one adder as a component of the arithmetic logic unit, wherein forming the at least one adder includes:

forming a sparse carry-merge circuit adapted to generate a group of carries,

forming a plurality of intermediate carry generators each coupled to the sparse carry-merge circuit and adapted to generate additional carries missing from the group of carries, and

forming a plurality of conditional sum generators coupled to the sparse carry-merge circuit and the plurality of intermediate carry generators and adapted to provide the sum of the two binary numbers.

34. The method of claim 33, wherein forming the sparse carry-merge circuit comprises forming a plurality of stages, each stage including a plurality of carry-merge logic gates to combine adjacent outputs from a preceding stage to provide the group of carries.

35. The method of claim 33, wherein forming each of the plurality of intermediate carry generators comprises forming three stages of ripple-carry merge gates.

36. The method of claim 33, wherein forming each of the conditional sum generators comprises:

forming four dual rail sum circuits; and

forming a multiplexer coupled to each dual rail sum circuit.

37. The method of claim 33, further comprising:

forming a multiplexer recovery circuit coupled to the sparse carry-merge circuit, each of the plurality of intermediate carry generators and each of the plurality of conditional sum generators.